UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,654	10/07/2003	Guan-Chyun Hsieh	DEE-PT133	7268

3624 7590 10/20/2004

VOLPE AND KOENIG, P.C.
UNITED PLAZA, SUITE 1600
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103

EXAMINER	
LAXTON, GARY L	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,654	HSIEH ET AL.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 9-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Divan (US 5,099,410).

Divan discloses an inverter for converting a DC input voltage into an AC output using a sigma-delta modulation (SDM), comprising: a sigma-delta modulation (SDM) controller (figure 8) for producing a modulated output voltage signal according to a reference voltage signal; a driving circuit (100, 101) electrically connected to the SDM producing a driving signal according to the modulated output voltage signal; and a power inversion stage circuit (53, 54) electrically connected to driving circuit (100, 101) for producing the AC output voltage according to the driving signal; wherein the power inversion stage circuit (53, 54) comprises: a power stage circuit electrically connected to the driving circuit (100, 101) for producing a AC power signal according to the driving signal and the DC input voltage; and a filter circuit (36, 37) electrically connected to the power stage circuit for producing the AC output voltage according to the AC power signal. The filter circuit is a low-pass filter. And comprises an inductor and a capacitor in series.

5. Claims 1 and 9-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Pearson (US 6,717,392).

Pearson discloses an inverter (figure 4) for converting a DC input voltage into an AC output using a sigma-delta modulation (SDM), comprising: a sigma-delta modulation (SDM)

controller (e.g. figures 2 or 3) for producing a modulated output voltage signal according to a reference voltage signal; a driving circuit (13) electrically connected to the SDM producing a driving signal according to the modulated output voltage signal; and a power inversion stage circuit (14) electrically connected to driving circuit (13) for producing the AC output voltage according to the driving signal; wherein the power inversion stage circuit (14) comprises: a power stage circuit electrically connected to the driving circuit (13) for producing a AC power signal according to the driving signal and the DC input voltage; and a filter circuit (16) electrically connected to the power stage circuit for producing the AC output voltage according to the AC power signal. The filter circuit is a low-pass filter. And comprises an inductor and a capacitor in series. The power stage circuit is in a full-bridge H-diagonal configuration comprising four MOSFET power switches (figure 4).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-8 and 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pearson (US 6,717,392) in combination with Divan (US 5,099,410).

Claims 2-8; Pearson discloses the claimed subject matter in regards to claim 1 supra, and further discloses the SDM controller comprises: an integrator circuit for producing an integrator output signal according to a difference between the reference voltage signal and the modulated

output voltage signal; and a quantizer circuit electrically connected to an input terminal of the integrator circuit through an output terminal thereof for quantizing the integrator output signal and producing the modulated output voltage signal.

However, Pearson does not disclose a sample-and-hold circuit connected to the integrator circuit for sampling and holding the integrator output signal.

Divan teaches an exemplary sigma delta modulator implementation (figure 8) which includes a sample and hold circuit (109) and an integrator circuit (106) in order to provide a circuit having limited ride through with passive energy storage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the controller of Pearson to include a sample and hold circuit connected to the integrator circuit in order to sample and hold the output signal from the integrator circuit in order to provide a circuit having limited ride through with passive energy storage as taught by Divan (col. 8 lines 56-68; col.. 9 lines 1-25 and lines 34-36).

Claims 17-25; Pearson discloses a controller (e.g. figures 2 or 3) for producing a modulated output voltage signal according to a reference voltage signal, comprising: an integrator circuit (20, 22, 23) for producing an integrator output signal according to a difference between the reference voltage signal and the modulated output voltage signal; and a quantizer circuit electrically to an input terminal of the integrator circuit through an output terminal thereof for quantizing output signal and producing the modulated output voltage signal.

However, Pearson does not disclose a sample-and-hold circuit connected to said integrator circuit for sampling and holding said integrator output signal.

Divan teaches an exemplary sigma delta modulator implementation (figure 8) which includes a sample and hold circuit (109) and an integrator circuit (106) in order to provide a circuit having limited ride through with passive energy storage.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the controller of Pearson to include a sample and hold circuit connected to the integrator circuit in order to sample and hold the output signal from the integrator circuit in order to provide a circuit having limited ride through with passive energy storage as taught by Divan (col. 8 lines 56-68; col.. 9 lines 1-25 and lines 34-36).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/15/04

Gary L. Laxton
Patent Examiner
Art Unit 2838